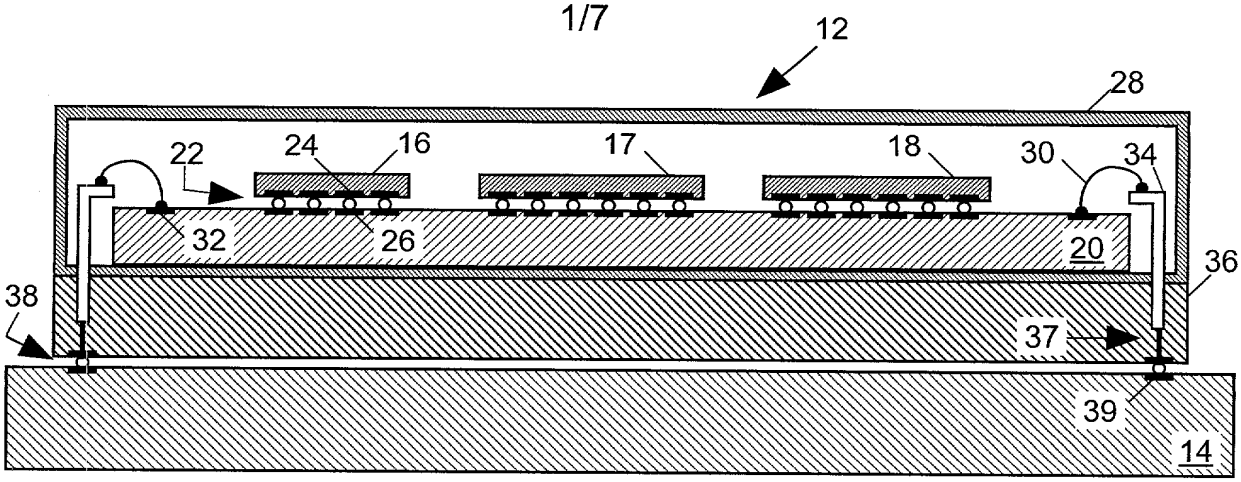

FIG. 1
(PRIOR ART)

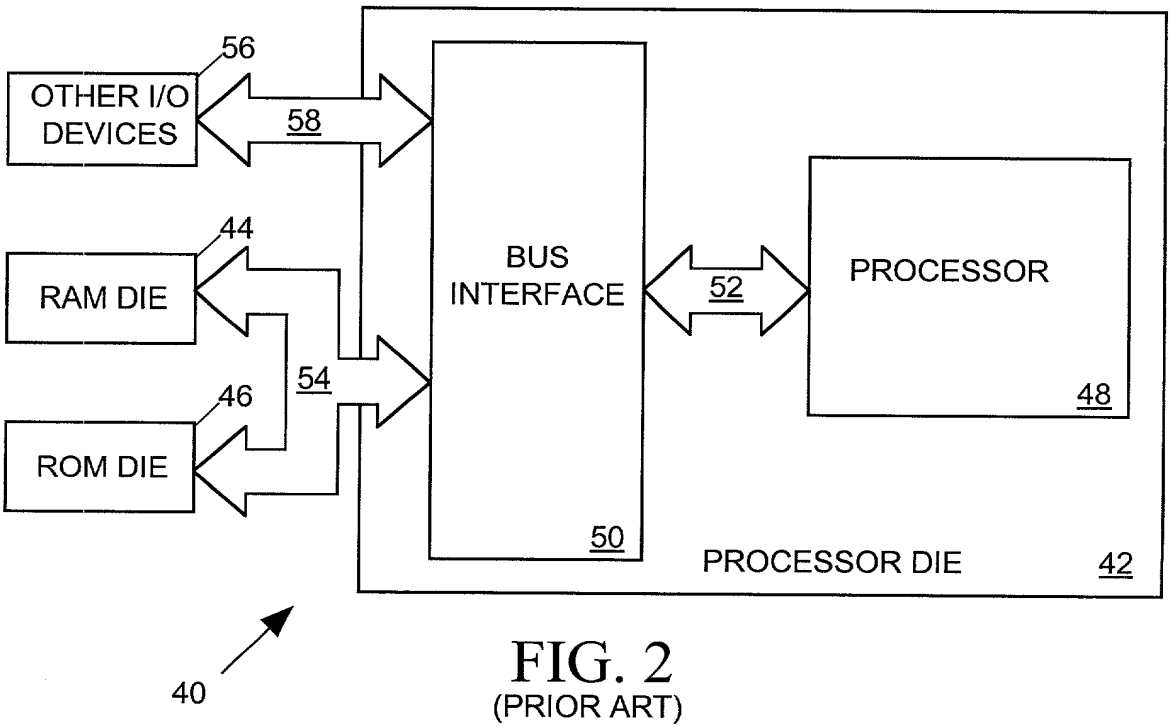

FIG. 2
(PRIOR ART)

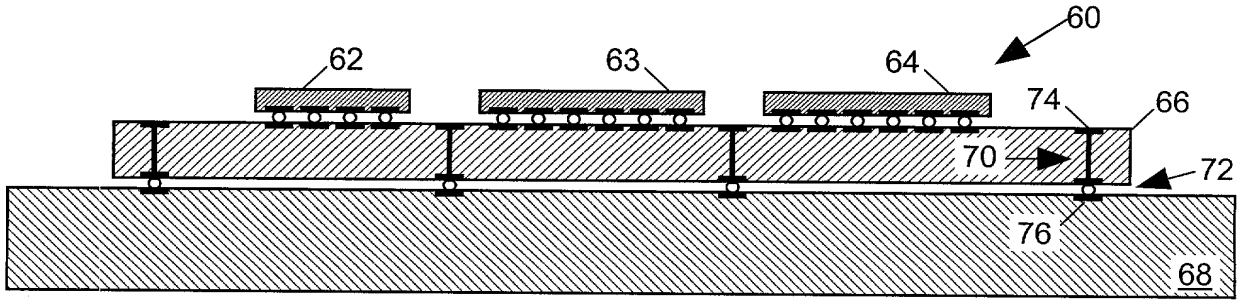

FIG. 3
(PRIOR ART)

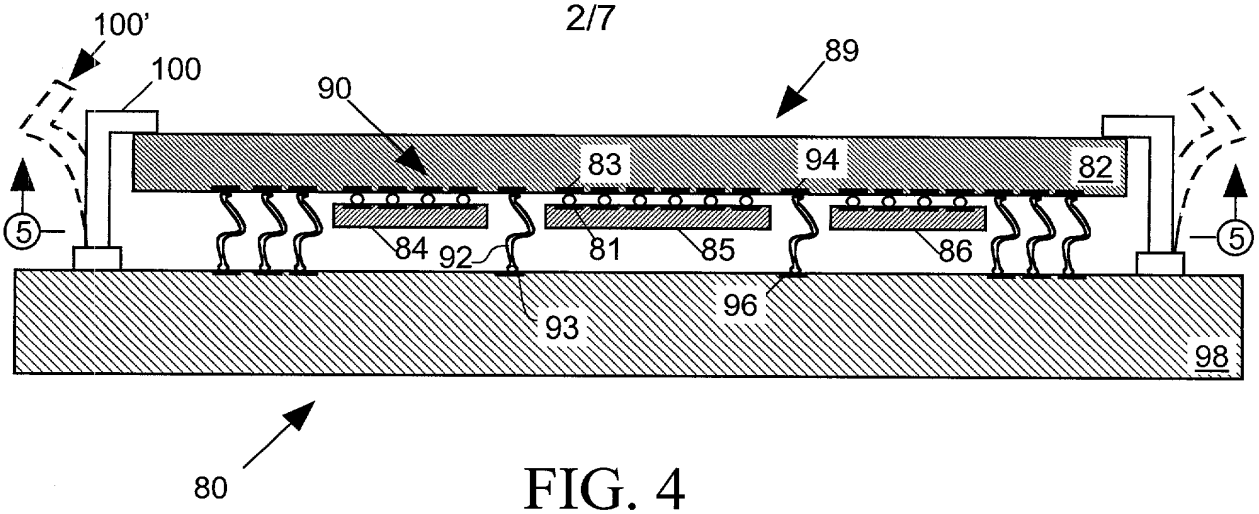

FIG. 4

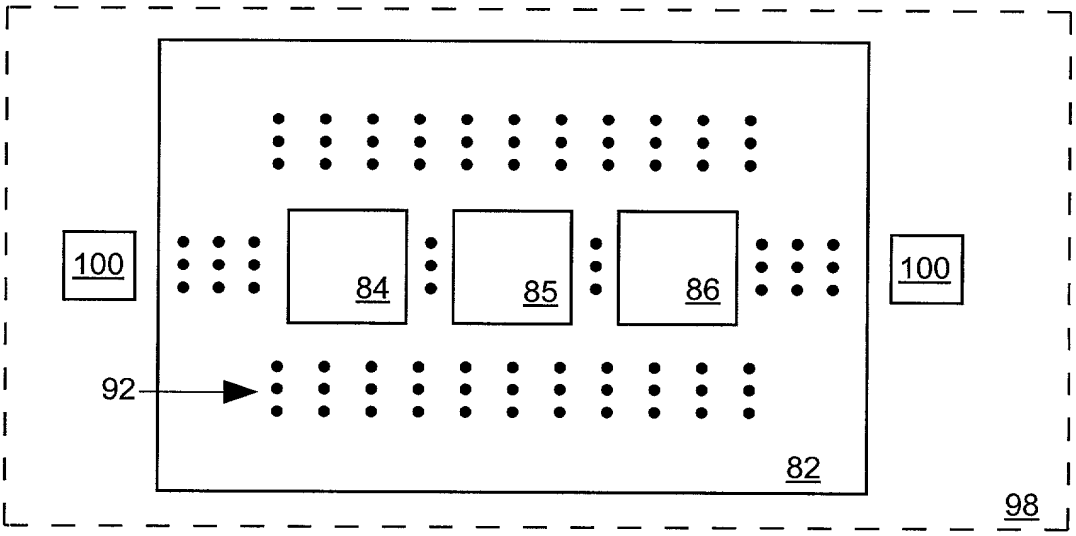

FIG. 5

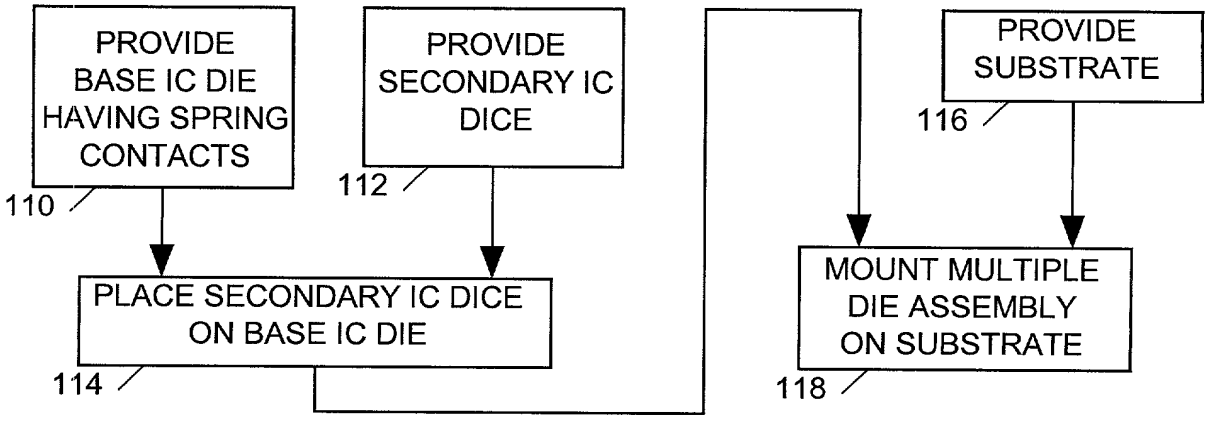

FIG. 6

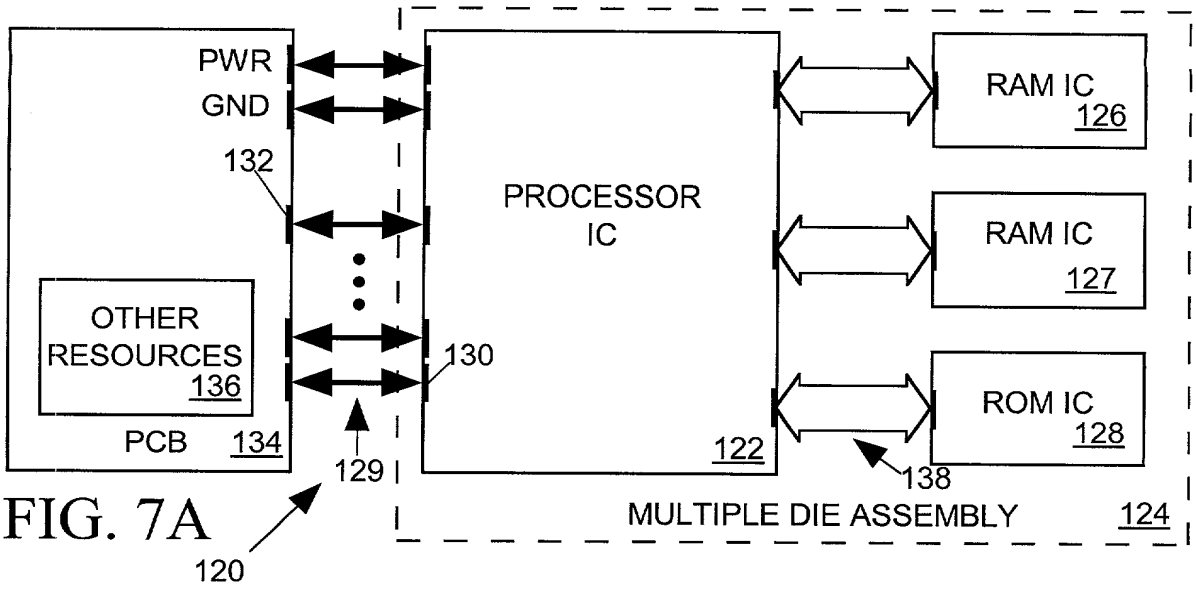

FIG. 7A

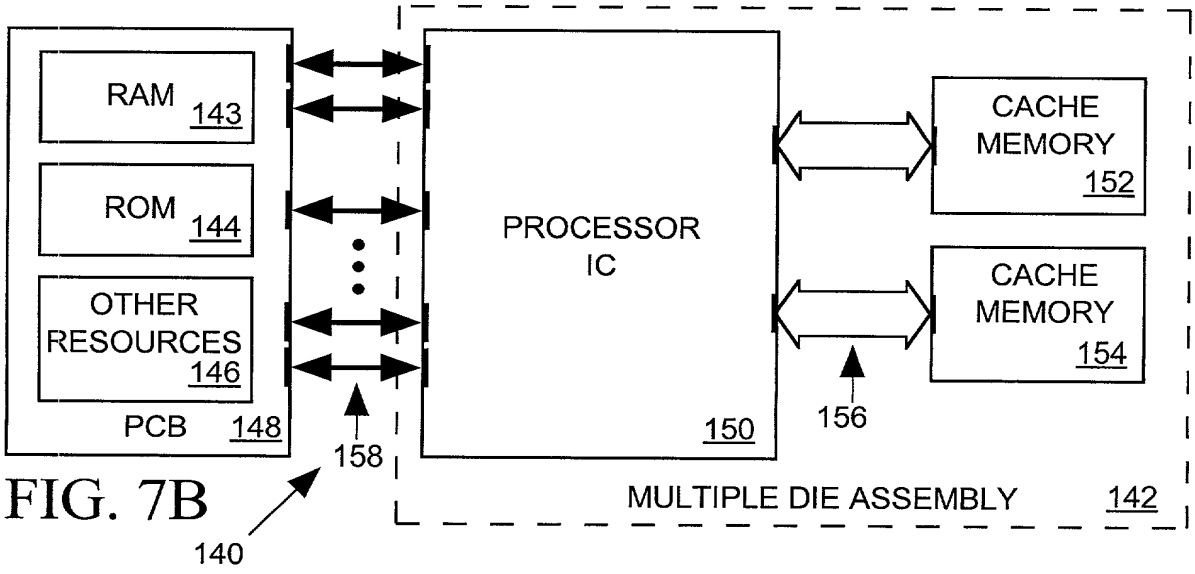

FIG. 7B

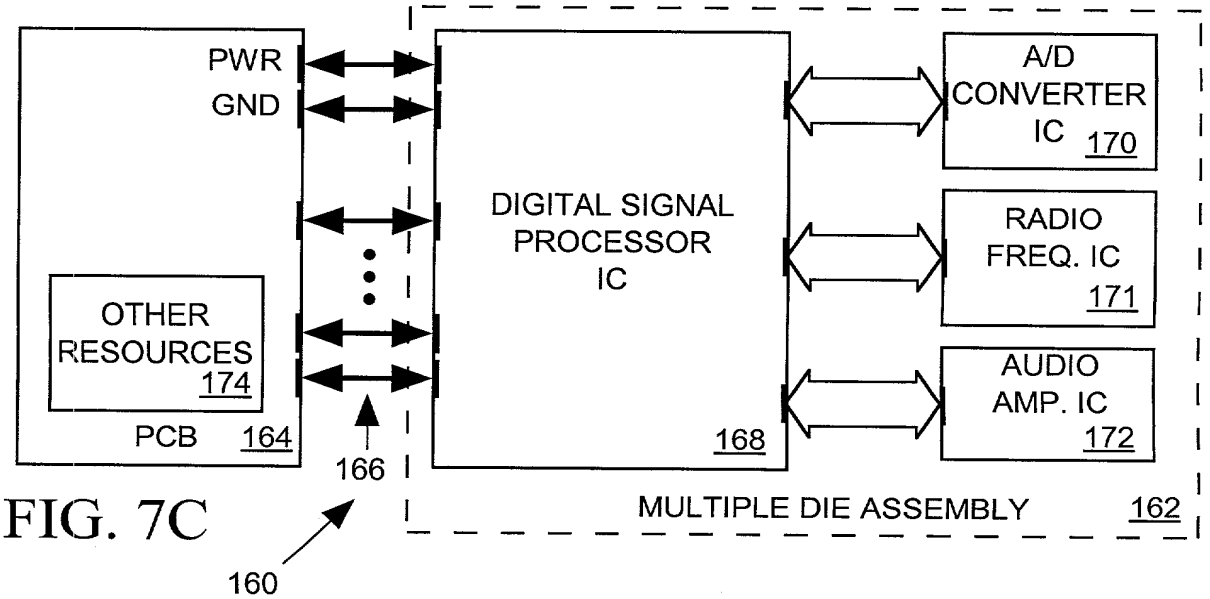

FIG. 7C

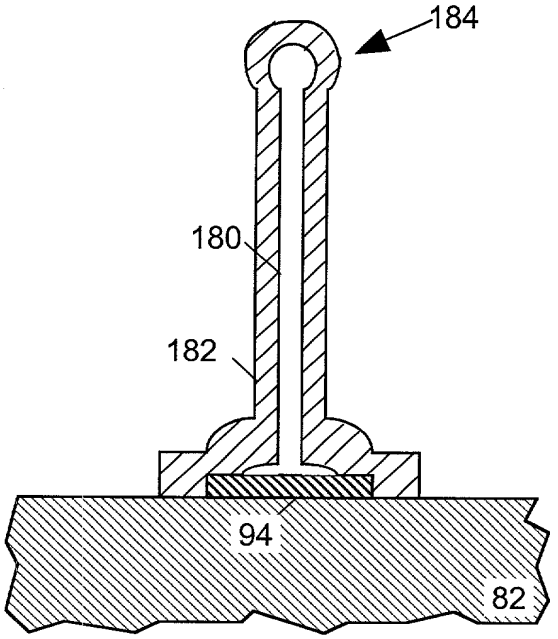

FIG. 8A

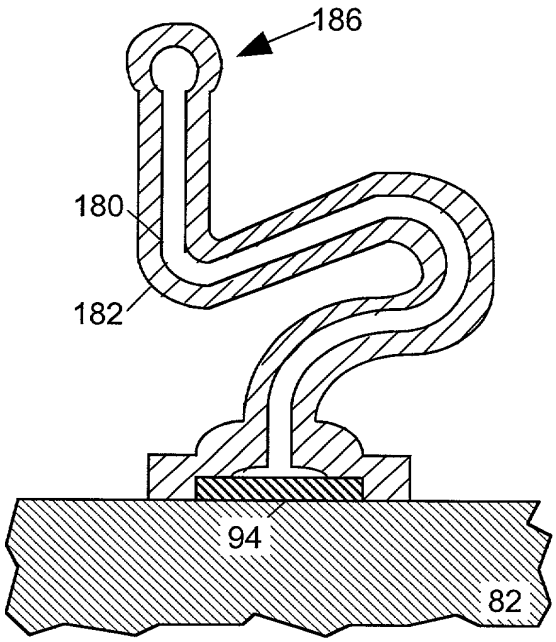

FIG. 8B

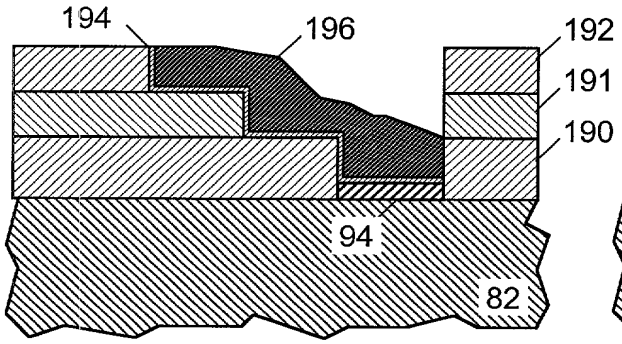

FIG. 9A

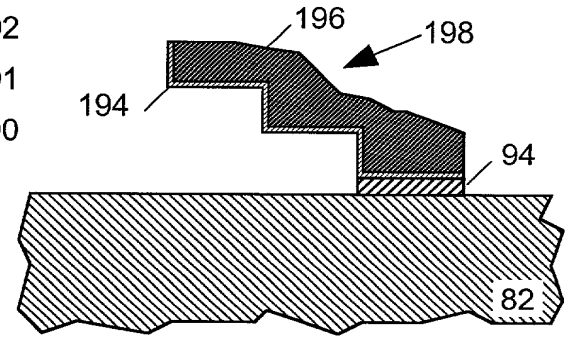

FIG. 9B

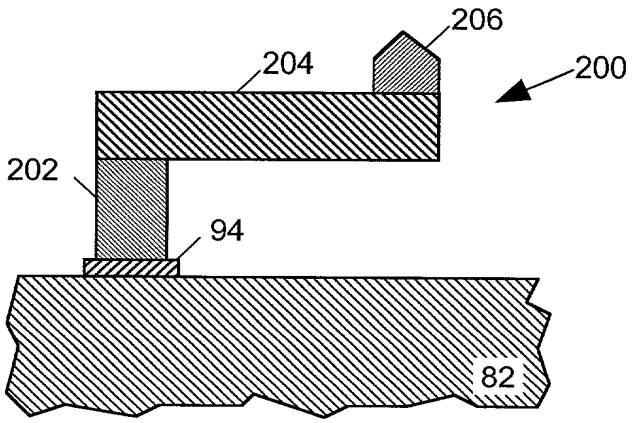

FIG. 10

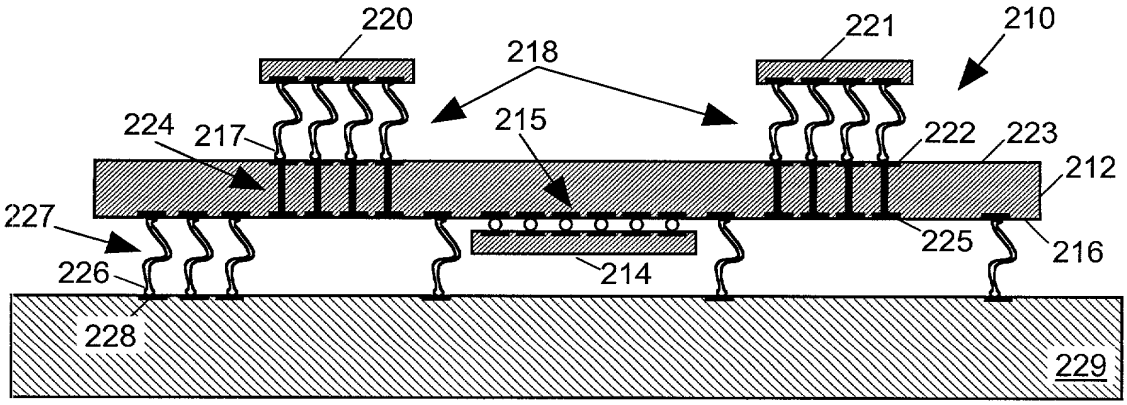

FIG. 11

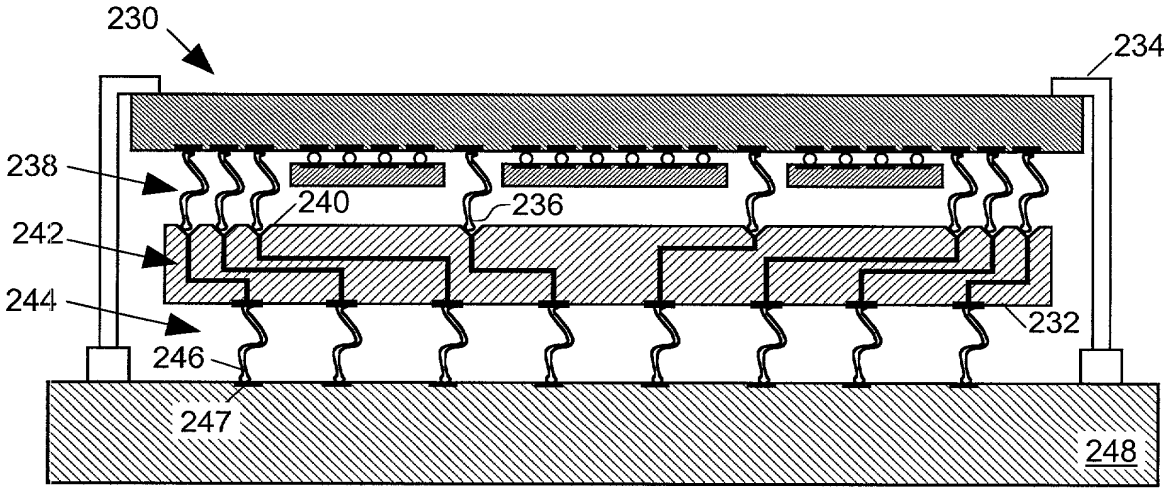

FIG. 12

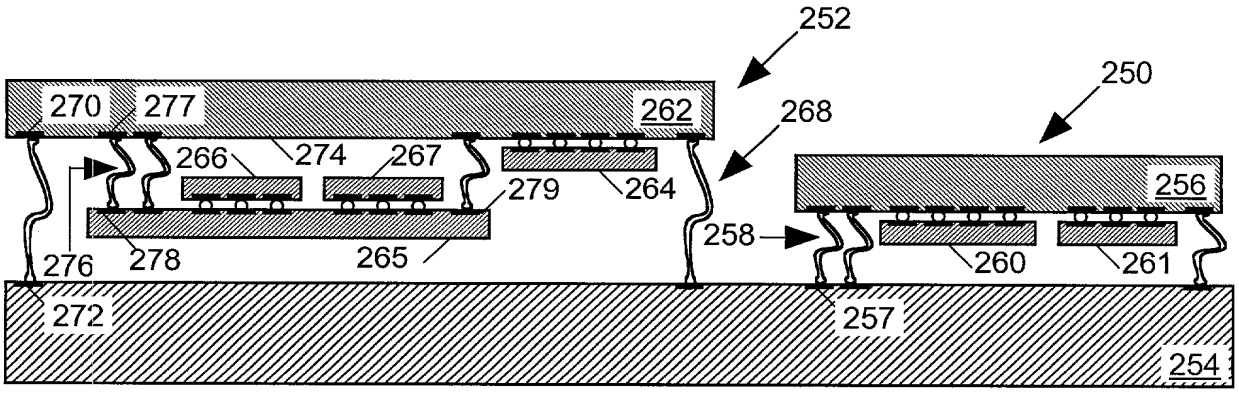

FIG. 13

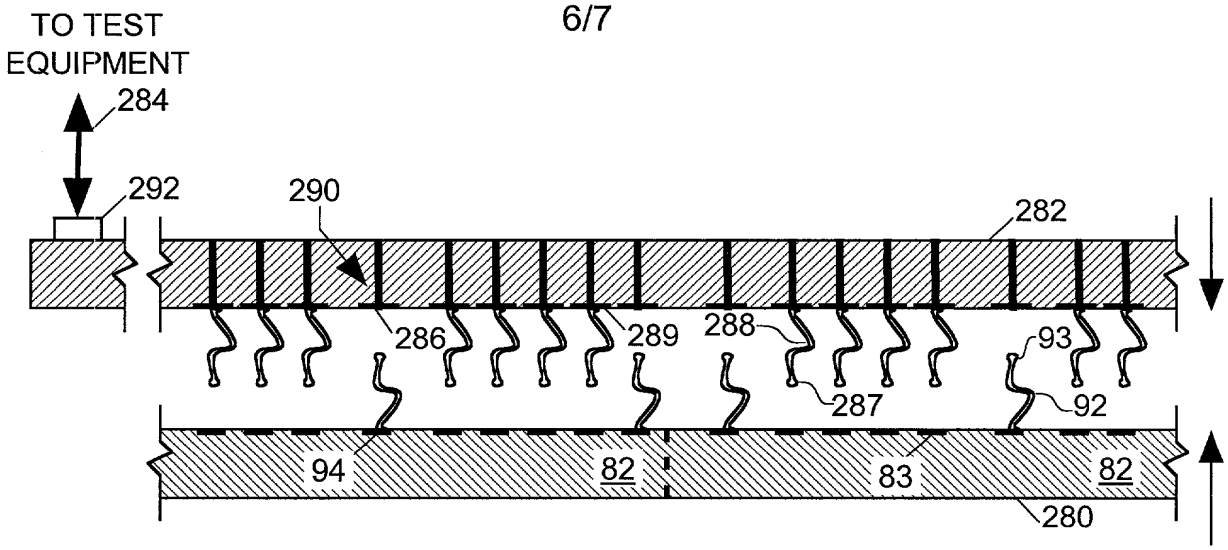

FIG. 14A

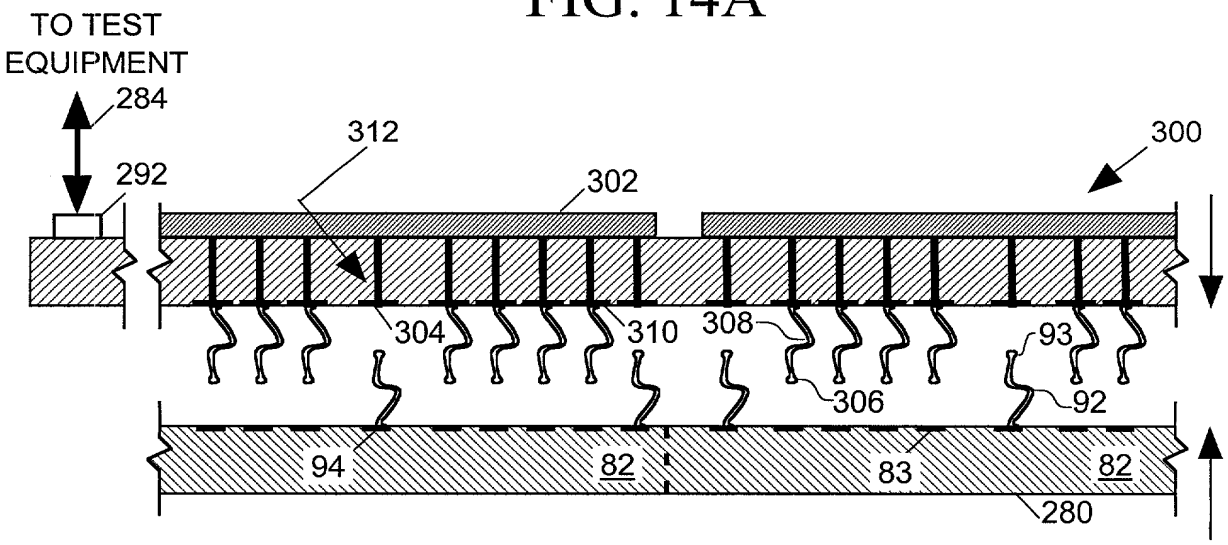

FIG. 14B

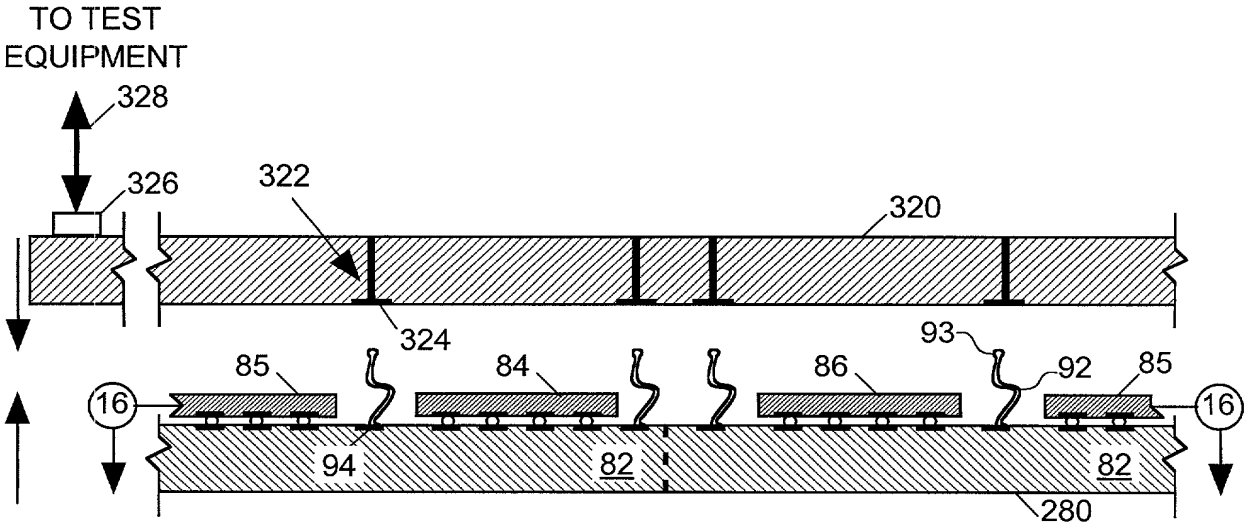

FIG. 15

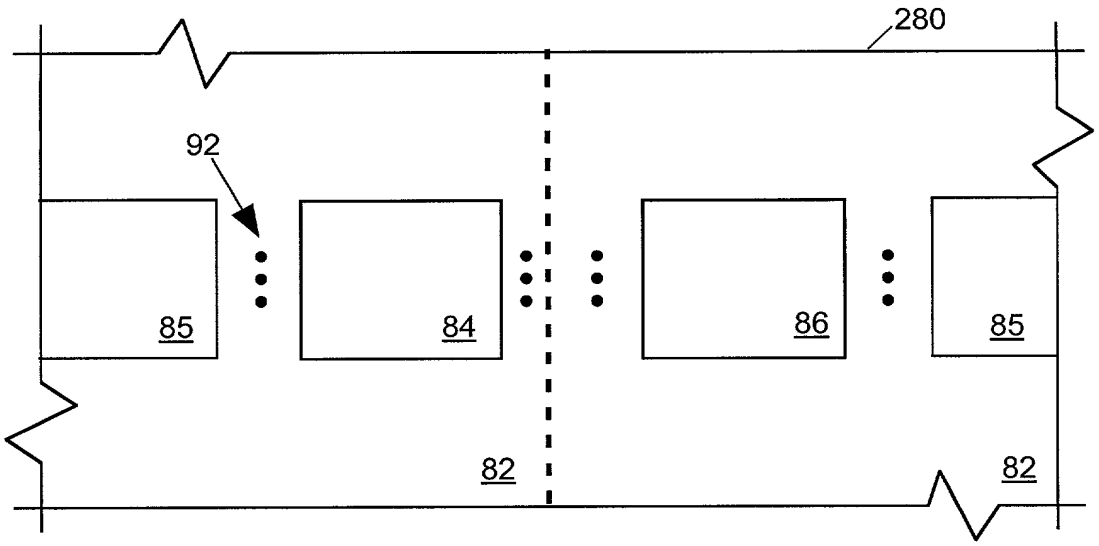
280
92
85
84
86
85
82
82

FIG. 16

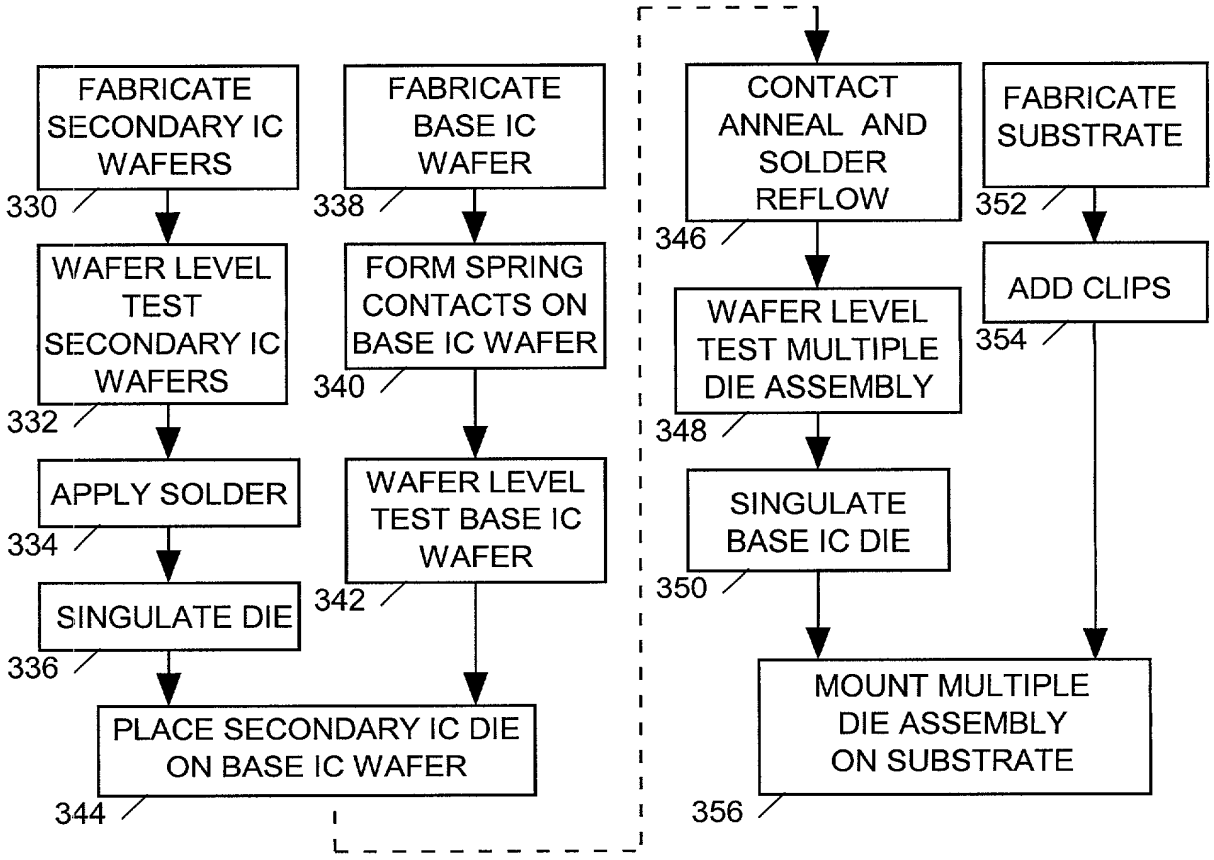
FABRICATE SECONDARY IC WAFERS
330
WAFER LEVEL TEST SECONDARY IC WAFERS
332
APPLY SOLDER
334
SINGULATE DIE
336
FABRICATE BASE IC WAFER
338
FORM SPRING CONTACTS ON BASE IC WAFER
340
WAFER LEVEL TEST BASE IC WAFER
342
PLACE SECONDARY IC DIE ON BASE IC WAFER
344
CONTACT ANNEAL AND SOLDER REFLOW
346
WAFER LEVEL TEST MULTIPLE DIE ASSEMBLY
348
SINGULATE BASE IC DIE
350
FABRICATE SUBSTRATE
352
ADD CLIPS
354
MOUNT MULTIPLE DIE ASSEMBLY ON SUBSTRATE
356

FIG. 17